CLAIMS

1. (Currently amended) A read only memory device, comprising:

a read only memory cell array including:

a plurality of first read only memory cells coupled to ~~a~~ the plurality of word lines, a plurality of first bit lines, and a plurality of first virtual ground lines; and

a plurality of second read only memory cells coupled to ~~a~~ the reference word line, a plurality of second bit lines and a plurality of second virtual ground lines;

a reference memory cell array including:

a plurality of first reference memory cells coupled to a plurality of dummy word lines, at least one reference bit line, and at least one reference virtual ground line; and

at least one second reference memory cell coupled to the reference word line, the at least one reference bit line, and the at least one reference virtual ground line; and

a dummy memory cell array including:

a plurality of first dummy memory cells coupled to the plurality of dummy word lines, at least one dummy bit line, and at least one dummy virtual ground line; and

~~a plurality of~~ at least one second dummy memory cells coupled to the reference word line, the at least one dummy bit line, and the at least one dummy virtual ground line;

where the reference word line is selected when at least one of the plurality of word lines is selected.

2. (Currently amended) The device of claim 1 ~~where the reference word line is selected responsive to the plurality of word lines~~ comprising:

a row decoder to decode a plurality of word lines responsive to an address;

a reference word line selecting circuit to generate a reference word line responsive to the address, the reference word line selecting circuit being distinct from the row decoder.

3. (Currently amended) The device of claim ~~1~~ 14

where the plurality of dummy word lines is ~~coupled~~ connected to the plurality of word lines; and

where the plurality of first dummy memory cells are programmed to data "1."

4. (Currently amended) The device of claim ~~1~~ 14

where the plurality of dummy word lines is ~~coupled~~ connected to a power voltage; and

where the plurality of first dummy memory cells are programmed to data "1."

5. (Currently amended) The device of claim ~~1~~ 14 where the plurality of dummy word lines is ~~coupled~~ connected to a ground voltage.

6. (Currently amended) The device of claim ~~1~~ 14

where the plurality of ~~dummy word lines~~ of second bit lines and the plurality of second virtual ground lines is ~~coupled~~ permanently connected to the plurality of word lines; and

where the plurality of first reference memory cells are programmed to data "1."

7. (Currently amended) The device of claim ~~1~~ 14

where the plurality of second bit lines is coupled to the plurality of first bit lines; ~~and~~

where the plurality of second virtual ground lines is coupled to the plurality of first virtual ground lines; and

where the plurality of second read only memory cells is programmed to a data "1."

8. (Currently amended) The device of claim ~~1~~ 14 comprising a MOS transistor having a gate coupled to the reference word line.

9. (Currently amended) The device of claim ~~1~~ 14 where the read only memory cell array includes an NMOS transistor having a gate coupled to the reference word line.

10. (Currently amended) The device of claim ~~1~~ 14 where the at least one second reference memory cell includes an NMOS transistor.

11. (Currently amended) The device of claim ~~1~~ 14 where the at least one second dummy memory cell includes an NMOS transistor.

12. (Currently amended) A read only memory device, comprising:

a read only memory cell array including:

a plurality of first read only memory cells coupled to a plurality of word lines, a plurality of first bit lines, and a plurality of first virtual ground lines; and

a plurality of second read only memory cells coupled to a reference word line, a plurality of second bit lines, and a plurality of second virtual ground lines;

a reference memory cell array including:

a plurality of first reference memory cells coupled to a plurality of dummy word lines, at least one reference bit line, and at least one reference virtual ground line; and

a plurality of second reference memory cells coupled to the reference word line, the at least one reference bit line, and the at least one reference virtual ground line; and

a dummy memory cell array including:

a plurality of first dummy memory cells coupled to the plurality of dummy word lines, at least one dummy bit line, and at least one dummy virtual ground line; and

a plurality of second dummy memory cells coupled to the reference word line, the at least one dummy bit line, and the at least one dummy virtual ground line;

a row decoder to decode a row address that selects the plurality of word lines;

a reference word line selecting circuit to select a reference word line responsive to the row address;

a first column decoder and virtual ground line selecting circuit to decode a column address that selects the plurality of bit lines and the plurality of the first virtual ground lines; and

a second column decoder and virtual ground line selecting circuit to select the at least one reference bit line and the at least one dummy bit line responsive to the column address;

where the reference word line selecting circuit selects the reference word line when at least one of the plurality of word lines is selected.

13. (Original) The device of claim 12 where the reference word line selecting circuit decodes predetermined bits of the row address.

14. (New) The device of claim 2

where at least one second reference memory cell is programmed to data "0;" and

where the at least one second dummy memory cell is programmed to data "0."

15. (New) The device of claim 14

where the plurality of dummy word lines is connected to a power voltage; and

where the plurality of first reference memory cells is programmed to a data "1."

16. (New) The device of claim 14 where the plurality of dummy word lines is connected to a ground voltage.

17. (New) The device of claim 14 the reference word line selecting circuit comprises:

a decoder to decode a portion of the address; and

a logic circuit to logically manipulate the decoded portion of the address from the decoder.

18. (New) The device of claim 12 where the reference word line selecting circuit includes:

a decoder to decode a portion of the row address to output decoding signals; and

a logic circuit to logically manipulate the decoding signals.